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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,446	08/26/2003	Kazuhiro Aoshima	1076.1089	1651

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EXAMINER	
SIDDIQI, MOHAMMAD A	
ART UNIT	PAPER NUMBER
2154	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/647,446	AOSHIMA, KAZUHIRO	
	Examiner	Art Unit	
	Mohammad A. Siddiqi	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/26/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 8/26/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/24/03,10/05/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for the examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 12/24/2003 and 10/05/2006 has been considered by the examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Regarding claims 9, 14 and 18-20 , the phrase " substantially the same " renders the claim indefinite because it is unclear it fails to point out what is included or excluded by the claim language. See Ex parte Fressola, 27 USPQ2d 1608 (Bd. Pat. App. & Inter. 1993).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishida et. al. (S 2002/0167851) (hereinafter Ishida).

7. As per claim 1, Ishida discloses a data processor for communicating data to and from a host computer via an interface with a packet including a packet ID (fig 1A, page 3, para #0073), the data processor comprising: a packet recognition circuit for receiving the packet including the packet ID (fig 1B) from the host computer (fig 1A) and recognizing the type of the packet from the packet ID (fig 1B, page 4, para #0080); and a packet length (page 2, para #0045) measuring circuit connected (page 3, para #0073; fig 3, page 4 , para #0080) to the packet recognition circuit for measuring packet length of the packet received from the host computer (fig

1A) and determining whether the measured packet length (fig 3, page 2, para #0045) is in accordance with the packet type (data transfer type, page 3, para #0073; fig 3, page 4 , para #0080) to recognized by the packet determination circuit (fig 3, page 4 , para #0080).

8. As per claim 2, Ishida discloses the packet length measuring circuit generates a suspension signal for suspending data transfer from the data processor to the host computer when the measured packet length is not in accordance with the packet type (data transfer type, page 3, para #0073; fig 3, page 4, para #0080).

9. As per claim 3, Ishida discloses the interface includes a USB interface (fig 1A, page 3, para #0067).

10. As per claim 4, Ishida discloses a data processor for communicating data to and from a host computer via an interface (fig 1A), the data processor comprising: a plurality of end points (host, device, Fig 1A, page 3, para #0070), each processing a transaction corresponding to a data transfer request from the host computer (host Fig 1A, page 3, para #0070), wherein each of the end points stores a data toggle bit (toggle bit, fig 17A-17B) having a value that is inverted whenever a predetermined packet from the

host computer is received (toggle bit, fig 17A-17B); and a toggle bit switching circuit connected to the end points to determine whether a first end point (page 2, para #0044-#0049) that received a transfer request in a previous transaction and a second end point that received a transfer request in the present transaction are substantially the same (toggle bit, fig 17A-17B, page 2, para #0044-#0049), wherein the toggle bit switching circuit inverts the value of the data toggle bit stored (toggle bit, fig 17A-17B) in the first end point when the first end point differs from the second end point (page 2, para #0044-#0049).

11. As per claim 5, Ishida discloses each end point has an end point number, and the predetermined packet includes the end point number (page 2, para #0044_#0049); and the toggle bit switching circuit includes an end point storage section for storing the end point number included in the predetermined packet transmitted from the host computer (fig 1A) and determines whether the first and second end points are substantially the same by comparing the end point number of the first end point stored in the storage section with the end point number of the second end point (page 2, para #0044_#0049).

12. As per claim 6, Ishida discloses the interface includes a USB interface, and the end point is included in a token packet (Page 3, para #0067).

13. As per claim 7, Ishida discloses the toggle bit switching circuit inverts the data toggle bit value of the first end point when receiving a handshake packet from the host computer (toggle bit, fig 17A-17B, page 2, para #0044-#0049).

14. As per claim 8, Ishida discloses the interface includes a USB interface (Page 3, para #0067).

15. As per claim 9, Ishida discloses a data processor for communicating data to and from a host computer via a predetermined interface with a packet including a packet ID (fig 1A, page 3, para #0073), the data processor comprising: a packet recognition circuit for receiving the packet including the packet ID from the host computer and recognizing the type of the packet from the packet ID (fig 1B, page 4, para #0080);

a packet length measuring circuit connected to the packet recognition circuit for measuring packet length of the packet received from the host computer (fig 3, page 2, para #0045) and determining whether the measured packet length is in accordance with the packet type recognized by

the packet determination circuit (data transfer type, page 3, para #0073; fig 3, page 4, para #0080);

a plurality of end points (host, device, Fig 1A, page 3, para #0070), each processing a transaction corresponding to a data transfer request from the host computer (page 2, para #0044-#0049), wherein each of the end points stores a data toggle bit (toggle bit, fig 17A-17B) having a value that is inverted whenever receiving a predetermined packet from the host computer (page 2, para #0044-#0049); and a toggle bit (toggle bit, fig 17A-17B) switching circuit connected to the end points to determine whether a first end point that received a transfer request in a previous transaction and a second end point that received a transfer request in the present transaction are substantially the same (page 2, para #0044-#0049), wherein the toggle bit (toggle bit, fig 17A-17B) switching circuit inverts the value of the data toggle bit stored in the first end point when the first end point differs from the second end point (page 2, para #0044-#0049).

16. As per claim 10, Ishida discloses the interface includes a USB interface Page 3, para #0067).

17. As per claim 11-13, claims are rejected for the same reasons as claims 1-3, above.

18. As per claim 14-17, claims are rejected for the same reasons as claims 4-8, above.

19. As per claim 18-20, claims are rejected for the same reasons as claims 4-9, above.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 6,816,929

U.S. Patent 6,760,795

U.S. Patent 6,760,772

U.S. Patent 6,757,783

U.S. Patent 6,742,076

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad A. Siddiqi whose telephone number is (571) 272-3976. The examiner can normally be reached on Monday -Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MAS

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